Reliability of Micro-vias in Flex Based Materials

James Keating, Robert Larmouth
Teledyne Electronic Technologies
110 Lowell Road
Hudson, NH 03051
Phone: (603) 889-6191 FAX (603) 882-4457

Abstract

Space limitations are forcing electronic packages to have increasingly higher densities. Packaging options such as MCM-L are gaining in popularity as lower costs are required for consumer products. With these increases in circuit density come the need for smaller feature sizes on the substrate. One solution to the circuit density requirement is to reduce the diameter of the via and the associated pad at the design phase, but still maintain producibility at board fabrication.

This paper will describe and compare two methods of producing micro-vias in laminate based materials. Data collected to date that compares the two methods will be presented to try to determine if there is a difference in the reliability of the laser versus plasma formed micro-via. An actual application for a tactical missile electronics module that incorporates micro-vias on flex based materials will be discussed along with how the micro-via approach helped accomplish the needed wiring density. Design rules for via diameter and pad diameter will be presented. Thermal cycling and thermal shock tests will be performed on a double-sided polyimide film based high density decal that represents wiring densities and techniques that will be employed in production. Test conditions and conclusions will be presented.

INTRODUCTION

The use of flexible circuitry has been steadily increasing in response to advances in the infrastructure and supplier chain. This type of circuitry, long used as a simple interconnect between electronic modules or rigid PC cards, is quickly becoming an industry unto itself. Many applications are being designed that require SMT on flex as well as Chip-on-flex (COF) and Flip Chip on Flex (FCOF). These types of electronic devices require increased density when compared to traditional pin in hole type components and rely heavily upon vias to create the electrical path to the inner layers. When compared to FR 4 epoxy resin laminates flex based materials offer factors such as improved electrical characteristics, the ability to more reliably create fine features, and they are amenable to a wider range of processing techniques.[1] Traditionally the size of a small diameter drilled via is 0.012" (0.30mm) diameter through an 0.020" (0.50mm) diameter pad. Using these types of circuit densities flex vendors have been able to accommodate packaged components with pitches as low as 0.025" (0.625mm). Some vendors have had success drilling holes as small as 0.008" (200µm) diameter in a 0.014" (0.35mm) diameter pad, in an attempt to increase circuit densities to allow for the use of newer packaging technologies such as BGAs.

However, package sizes are shrinking dramatically and many are not much larger than the chip itself. To conform to these smaller package sizes designers are being forced to increase board densities. One of the easiest ways to accomplish this is to further reduce feature sizes, including the via hole, and the associated capture pad diameter. Flex based materials lend themselves quite readily to micro-machining holes using a variety of processing techniques. This allows vendors many options when forming micro-vias, defined in this paper as holes less than or equal to 0.004" (100µm) in diameter.

MICRO-VIA HOLE FORMATION

Below are a number of techniques that can be employed to form micro-vias in flex based materials. They are listed in no set order of precedence or preference:

- *mechanical drilling*
- *mechanical punching*
- *photo-defined*
- *plasma ablation*
- *laser ablation*

There are many reasons a vendor may or may not choose a particular technique for via formation. Teledyne has experimented with mechanical drilling of small hole vias for some time and has had success in drilling holes as small as 0.008” (200µm) diameter using industry standard equipment and processes. In fact, mechanically drilling holes as small as 0.006” (150µm) diameter has been accomplished, but yields and throughput are questionable at this point. In this paper the authors discuss two processes which were evaluated for a specific application that required high density routing and micro-vias on flex based materials.

PLASMA ABLATION

The first technique evaluated was the formation of the micro-vias by plasma ablation using a modified desmear system. With the plasma ablation process the diameter of the through hole is determined by the size of openings that can be imaged and etched in the copper metal layer. These openings in the copper allow the base laminate insulation to be exposed to the plasma gases. It is necessary to align the two artworks with respect to each other within a very tight process window. This allows the vias to be formed in the correct location and with the desired result. Any misalignment of the artworks with respect to each other will cause the holes to have an irregular shape or result in no via being formed. Initial testing proved that vias sizes ranging from 0.006” (150µm) diameter down to 0.003” (75µm) diameter could be effectively formed and etched in 0.002” (50µm) polyimide film with predictable results. Armed with this information the plasma chamber was characterized by a carefully planned DOE study to identify the optimal process settings and parameters that would allow for the ablation of 0.004” (200µm) diameter vias in 0.012” (0.30mm) pads.

Some of the concerns with plasma ablation, from Teledyne’s perspective, were:

- *Tight artwork registration*
- *Higher processing temperatures*
- *Amount of etchback*
- *Shape of the hole wall*

Artwork Registration

The artwork registration problem resulted in a process that would not lend itself to volume manufacturing with existing systems. In the tests performed a direct correlation between the artwork registration and the size of the via that could be formed was observed. Artwork mis-registration of greater than 0.001” (25µm) resulted in a process that would only yield micro-vias 0.003” (75µm). Additional capitalization, process capability studies, and training of personnel would have to be realized before the process would be production ready.

Temperature

The plasma operation involves the introduction of a gas that is excited through an RF field. The process itself generates heat that is transferred to the sheets during via formation. The test panels were fabricated using a 0.002” (50µm) thick unreinforced polyimide film. During the test cycle a disturbing and unpredictable amount of material movement was noticed that resulted in increased difficulty when attempting to align several layers together to form a multilayer composite. Another detractor to the plasma ablation procedure was the amount of time required to process the panels through the chamber. A normal etchback cycle ranges from fifteen (15) to twenty (20) minutes. To ablate the micro-vias cycle times averaged around forty five (45) minutes, including a preheat and cool down cycle.

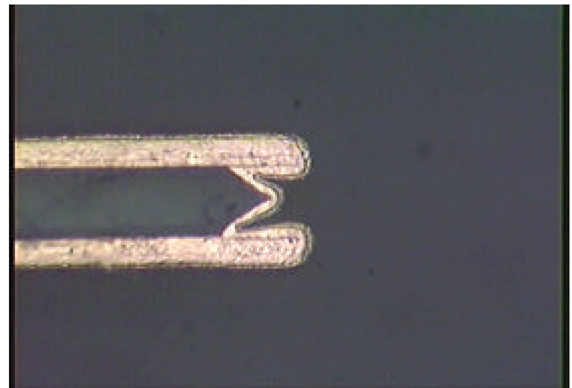

Figure 1

Typical Plasma Etched Micro-via.(200mm Æ via)

Etchback

The plasma method of forming holes is fairly self limiting. Once a via has been formed the ablation begins to slow down until there is no more exposed organic material. However, there is some undercutting of the film below the copper surfaces known as etchback that is normal and many times, for larger diameter holes in multilayer boards, quite desirable. For micro-vias the amount of etchback must be limited to not more than the thickness of the core laminate to prevent defects that may occur

when plating the via. This problem was somewhat solved by optimizing the process in such a way that the amount of etchback was limited, but never fully removed.

Via Shape
A normal by-product of the plasma etching process is an hourglass shape of the hole as shown in Figure 1. This is caused by the gases attacking the film from both sides until a through hole is formed. This phenomenon is quite normal for this operation. Although no reliability concerns were raised this was not the desired result.

Despite the process issues noted much success has been achieved using the plasma ablation procedure for forming micro-vias. Several test vehicles have been designed and manufactured and this process has been optimized to meet current needs. Circuit boards have been designed, produced and shipped to customers that successfully incorporated plasma etched vias to allow the necessary densities to be met. However, additional capitalization would be required to make the process attractive from a volume production perspective.

LASER ABLATION

There are several laser drilling technologies currently available to printed wiring board vendors. Teledyne evaluated two of these systems taking into account the availability of equipment and resources. The first laser system evaluated used excimer based technology. Excimer laser systems offer the user the capability of individually spot drilling holes through the copper/insulation substrate as well as area scanning pre-etched openings that have been previously photodefined. The difference is the throughput and the amount of energy needed to do the different tasks. Less energy is required with an increase in throughput when using area scanning. This technique allows multiple holes to be laser ablated by using the copper as the laser mask. The beam can be directed to a larger area allowing for the formation of several holes at one time. The amount of energy required to ablate the insulation material is less than the amount required to drill through a metal layer.

The other laser system evaluated was a CO_2 laser drilling system. Since this particular machine was specifically designed for laser drilling micro-vias in PCB's, improved throughput and process control were noticed. CO_2 lasers are not capable of drilling through a metal layer so openings must be photodefined and etched prior to processing. This limits the via diameter to the size opening that can be formed in the copper base material. However, the openings need only be formed on one side of the laminate. The problem of registering artwork front to back, as with the plasma process, was resolved.

Neither laser drilling operation introduced a high thermal rise for an extended period of time, so material movement problem encountered with the plasma process was not an issue. Both laser processes resulted in good through hole quality which required minimal cleaning to prepare the surface for plating. Figure 2 shows a typical laser ablated blind via. The hole wall is fairly uniform and does not exhibit the undercutting or hourglass shape normally found in a plasma etched hole.

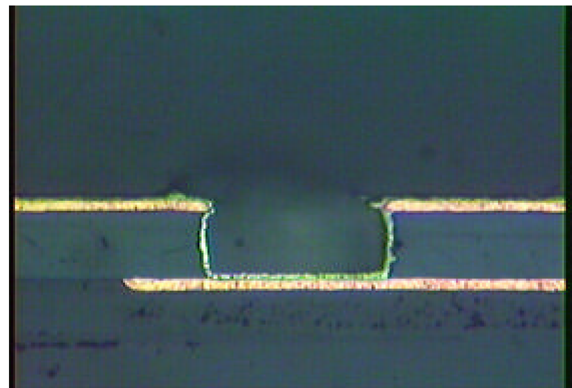

Figure 2
Typical Laser Etched Micro-via.(200mm Æ via)

The excimer laser ablated holes did have better visual quality than the holes formed using the CO_2 laser, but the holes were not evaluated for this from a reliability stand point. The CO_2 laser drilled holes required additional plasma cleaning for most of the materials evaluated but through conversations with material suppliers and the machine manufacturer it was learned that this is a function of the energy level and quite normal for this process. For cost and other reasons the laser drilled micro-vias evaluated for this project were all formed using a CO_2 laser drilling system and post cleaned using a CF_4 and O_2 plasma cleaning cycle.

DESIGN CONSIDERATIONS

Designers incorporating micro-via technology have to be aware of the fabricators ability to form not only the smaller diameter vias, but also to produce other feature sizes needed for advanced packages.

It may be possible to route three row devices, such as a pin grid array, in a single layer using 0.002” (50µm) lines and spacings but these fine pitch design rules are not used by most PWB and flex fabricators.[2] To design a circuit that is both manufacturable and has the area density to accommodate devices with a pitch below 0.020” (0.50mm) a redistribution layer would need to be incorporated. Circuit density could be further enhanced by the use of a via-in-pad concept. Using these techniques designs incorporating 0.010” (0.25mm) via land pads with 0.004” (200µm) vias can be produced using single track routing of 0.004” (100µm) lines with 0.003” (75µm) spacings.

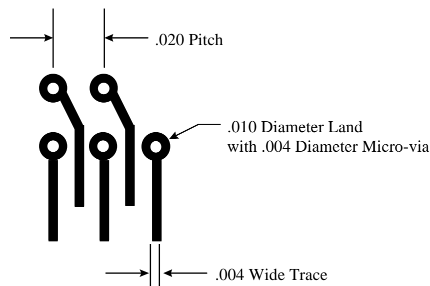

Figure 3
Single Track Routing on 0.020” (0.50mm) Centers

Using the above design rules Teledyne has manufactured test circuits that demonstrate the ability to support average pad densities of about 175 pads/in^2 and local densities up to 350 pads/in^2 with only two layers.[3]

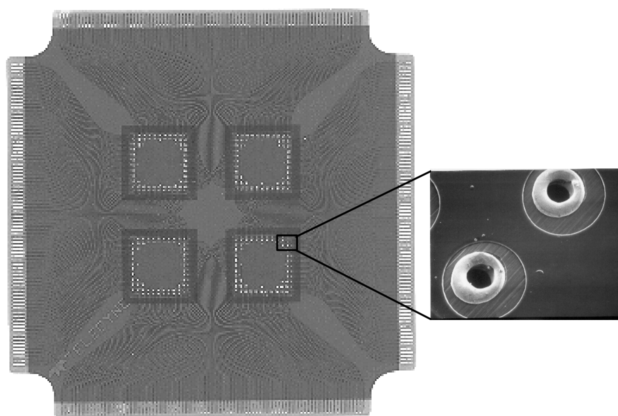

Figure 4
2 Layer High Density Test Circuit [3]

The above circuit incorporated a via-in-pad approach using 0.004” (100µm) vias within 0.010” (0.25mm) diameter pads. Line width and spacing was 0.003” (75µm) allowing for single track routing through the via field as explained above.

TODAY’S PACKAGING NEEDS

Design engineers are faced with challenges when incorporating state of the art electronics into their products. The phrase “lighter, faster and cheaper” is being universally applied to all market segments, including the military or high-end spectrum of packaging where traditionally performance, not reduced cost, was the focus for designing a product. Teledyne Electronics Technologies is well known in the military and aerospace marketplace for high reliability electronics packaging and is now seeing increasing demand for economically priced electronic packages, even in this established customer base. Several applications have been developed that transfer existing MCM-C modules to MCM-L technology which offer cost savings to the end user. One such application is in tactical missiles that now require lower cost as well as high density, high reliability, and thermal manageability.[4] Teledyne was contracted by a manufacturer of tactical missiles to produce a double sided circuit, or layered pair, that had relatively small features sizes. The intended end use of the layer pairs was to laminate several of these layers together to form a low cost multilayer substrate using a process called Colamination. This colamination process, offered by CTS Corporation, combines the aspects of all three MCM technologies: printed wiring board (L), thin film (D), and co-fired ceramic(C).[5]

In the colamination process, pads on two layered pairs are connected by means of a bond ply material containing sinterable vias in specific locations. During the lamination process, the copper-tin material in the bond ply via sinters together as well as the layered pair pads to form the electrical bond. It is believed that this configuration translates into the best density for dollar among competing substrate technologies.[4]

Teledyne’s role in this project is to manufacture the layered pair configurations that will be used in the colamination substrate. The design rules for the layered pair are as follows:

- *line and spacings: 0.002” (50**m**m)*
- *via pad diameter 0.005” (125**m**m)*
- *via diameter 0.002” (50**m**m)*
  (blind or plated closed)
- *via pitch 0.007” (175**m**m)*

The design required that the vias be plated shut or be formed as blind vias that would be open on one side only to assure that the CTS VIA-PLY™ material maintained electrical contact to the pad and did not flow through an opening in the substrate.

TEST VEHICLE DESIGN AND FABRICATION

Design

After reviewing the design requirements it was decided that the first evaluation necessary was to test the reliability of the via. Teledyne was contracted to manufacture a layered pair substrate which would incorporate the micro-vias-in-pad design technique. The test vehicle consisted of a daisy chained series of layer to layer interconnects. Feature sizes incorporated into the design were 0.010” (0.25mm) lines with 0.025” (0.625mm) pads. Via diameters chosen were both 0.003” (75μm) and 0.004” (100μm) to verify which via size had the highest producibility between the competing technologies. The design of the test vehicle is shown in Figure 5. The feature sizes chosen for line width and pad diameter did not represent the actual design requirement which was considerably denser. The test vehicle testing was specific and pertained to the reliability of the micro-via during thermal cycling. Other design features, such as the line widths and spacings, had been previously established and did not require further evaluation.

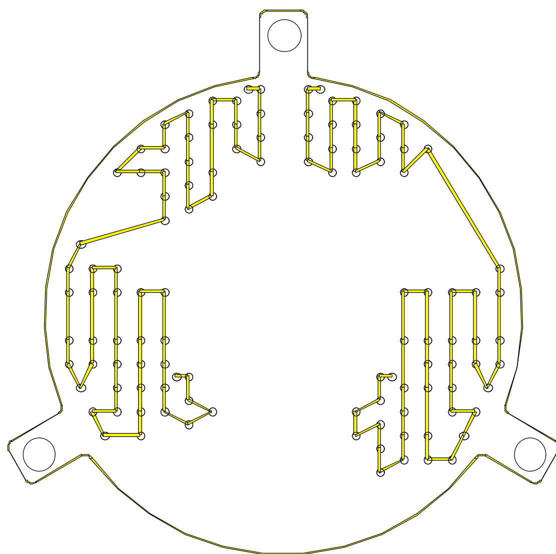

Figure 5
Two layer Daisy Chain Test Vehicle Artwork

Fabrication

The first manufactured lot utilized a plasma ablation approach to form the micro-via. Since the outcome of the plasma process is a through hole the vias would need to be plated shut to prevent the VIA-PLY™ material from flowing down the hole. Base film used for the test circuits was 0.002” (50μm) thick polyimide film (Kapton™) with ½ ounce (18μm) copper.

The circuits were imaged with a pad pattern artwork both top and bottom which allowed both 0.003 (75μm) and 0.004” (100μm) openings to be formed in the copper. The panels were then plasma etched to form the through hole micro-vias. The conductive image was transferred to the copper sheets using conventional photolithography. The micro-vias were plated closed using a standard electroless plating followed by electrolytic plate. A cross section of the plated shut via is shown in Figure 6 below. Although this process yielded the desired results there were some concerns with the reliability as well as the manufacturability of circuits using the plasma process.

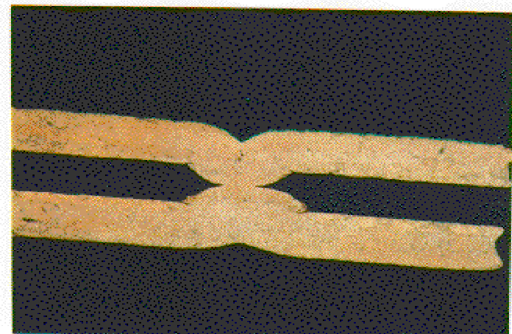

Figure 6
Cross section of Plated Shut 0.004” (100μm)
Plasma Etched Micro-via
(Photo Courtesy of Hughes Aircraft)

The same design was used to produce test circuits manufactured using laser ablation to form the micro-vias. A Lumonics CO_2 Laser Driller was used to form blind vias in the substrate. The material used for this evaluation was 0.002” (50μm) thick polyimide film clad with 7 micron copper. The thinner copper base will allow for the finer etch lines (0.002”) to be formed during production. The laminate was imaged on one side

with a pad pattern to allow copper to be etched to expose the laminate to the laser process. Both 0.003” (75µm) and 0.004” (100µm) diameter pads were imaged at this stage. Panels were laser drilled and then subsequently imaged and etched to form the daisy chain pattern. The laser ablated hole diameter corresponded with the diameter of the pre-etched openings in the copper. The holes formed were blind vias so there was no need to plate the vias closed. Through hole metallization was standard electroless deposition followed by electrolytic plating.

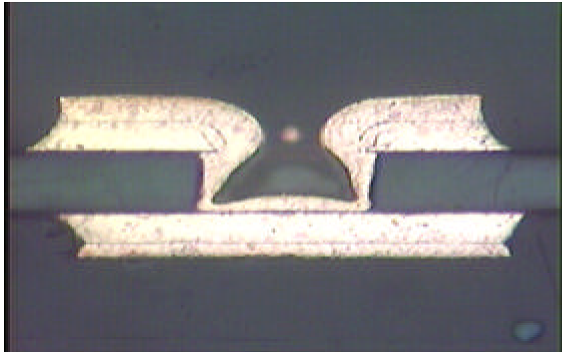

Figure 7
Cross section of Plated 0.004” (200µm)
Laser Etched Micro-via

RELIABILITY TESTING

The initial goal of the reliability testing was to evaluate the ability of a micro-via to withstand temperature cycling. When the decision was made to use more than one micro-via formation process the scope of the test was broadened to try to develop a comparison of the reliability differences, if any, between the two technologies. Hughes Aircraft performed the first round of thermal cycling tests so that their parameters would be documented and desired test conditions known for any subsequent testing.

Plasma Via Testing
The test requested involved thermally cycling the supplied sample daisy chain circuits while measuring the DC resistance. Each individual circuit was monitored for intermittent opens during the entire cycle. The temperature extremes were set at -55°C and + 125°C. Test sample size was nine (9) plated shut via circuit cards that each received 250 thermal cycles. Each test specimen had a daisy chained circuit on each side for a total of 18 circuits. Three of the samples tested received an additional 1750 thermal cycles bringing the total number of cycles to 2000 for these circuits.

During the test procedure approximately 100 milliamps of current flowed continuously through each daisy chain circuit. Resistance was measured and recorded during the testing. The circuits were monitored for intermittent opens, or high resistance increases, during each cycle. Each test specimen was subjected to 250 forced air thermal cycles at the following conditions:

- high temperature = + 125°C
- low temperature = - 55° C
- dwell time = 5 minutes @ temp.
- ramp rate = 15°C per minute

Three of the test specimens were subjected to another 750 cycles (1000 total) using the same temperature profile. These same three circuit cards were then subjected to an additional 1000 cycles of air-to-air thermal shock at the following conditions:

- high temperature = + 125°C
- low temperature = - 55° C
- dwell time = 5 min. @ temp.
- temperature transition time = 15°C per minute

Laser Via Testing
For comparative testing the laser drilled micro-via test circuit will also be thermally cycled to these same parameters. A customer has been supplied samples of the laser drilled daisy chain samples for evaluation and that data is forthcoming.

Teledyne will also be performing thermal reliability tests using the established test setup as a guideline for the parameters. The evaluation will consist of thermal cycling to the following guidelines:

- high temperature = + 125°C
- low temperature = - 55° C
- dwell time = 5 minutes @ temp.
- ramp rate = 15°C per minute

It is anticipated that a minimum of 100 cycles will be run using a forced air thermal cycling chamber. Additional testing of up to 1000 thermal cycles will be run to test the reliability of the via to withstand this harsh environment.

TEST RESULTS AND CONCLUSIONS

Plasma Vias

None of the test specimens showed any discontinuity during the initial 250 thermal cycles. The average DC resistance recorded for the low temperature range was 0.3 to 0.4 ohms. The resistance at high temperature was from approximately 0.6 to 0.8 ohms. Of the three circuit cards that were subjected to 2000 thermal cycles there was one legitimate failure. During the last phase of the thermal test one circuit began to show higher resistance (> 0.8ohms) at cycle 1769 during the high temperature portion of the test. The resistance increases continued for the remainder of the test cycle peaking at 424 ohms.

Test	Conditions	Result
Thermal Shock	550°F for 10 sec.	Pass
Thermal Cycle Phase I	-55°C to + 125°C 250 Cycles	Pass
Thermal Cycle Phase II	-55°C to + 125°C 1000 Cycles	Pass
Thermal Cycle Phase III (*)	-55°C to + 125°C 2000 Cycles	one failure @ 1769 cycles

* 1000 cycles temperature ramp rate 15°C per minute
1000 cycles temperature transition time 15°C per minute

Table 1
Thermal Reliability of Plasma Ablated Micro-vias

The initial concern regarding the thermal reliability of the plated closed plasma etched micro-via proved to be unfounded. Based on these results it can be stated that the plasma and plated shut micro-via approach will yield a robust layer to layer interconnect that is capable of passing hundreds and even thousands of thermal cycles without exhibiting electrical opens.

Laser Vias

To the first order, the reliability of micro-vias is a function of via diameter, copper plating properties, and the adhesion of the plating. Although geometry is somewhat different for the laser vias, the above variables are fairly consistent for both processes, therefore, the reliability of the laser formed micro-vias is expected to be comparable to the plasma formed vias. As mentioned earlier, this will be confirmed through additional thermal testing. Second order effects from the ablation processes themselves, such as the shape of the hole wall and elimination of etchback, will be evaluated during this phase of testing.

SUMMARY

As part of an effort to evaluate the reliability of micro-vias for this specific application, a tactical missile, the tests performed have provided valuable data that can be applied to any one of many micro-electronics packaging options currently available. The end user for this application was satisfied with the test results and will be designing this interconnection scheme into the product. This solution will allow for all of the performance requirements of the tactical missile to be met and decrease the overall package size resulting in a smaller and lighter end product. To date micro-vias have been designed into many applications such as chip scale packages, military electronics, and MCM-L designs that require enhanced densities. Design rules have been established that will allow for densities of at least 175 pads/in^2 to be met by incorporating the techniques outlined above without sacrificing producibility.

Previous modeling has been done that shows that the micro-via in pad design will improved the reliability for both flex and FR4 based substrates, allowing it to be considered for higher density routing designs.[6] The testing done to date and recorded here has proved that the micro-via with via-in-pad design approach is a very reliable electrical connection between multiple layers of flex circuitry.

Much work still needs to be done to optimize which particular micro-via technique may be best for a specific application or flex vendor. This decision may be based on a number of reasons such as:

- via diameter
- cost per hole
- blind via vs. buried via
- equipment cost
- volume …*etc.*

Additional testing that would result in defining the optimal plating thickness for micro-vias based on the via size or the plating process used (i.e. electroless deposition or direct metallization) would benefit vendors and end users alike.

Flexible circuit manufacturers will undoubtedly benefit from the amenability to wider ranges of processing techniques that flex base materials offer when choosing which process they will pursue.

REFERENCES:

[1] "Multilayer Flexible Circuits with Area Array Interconnections for High Performance Electronics" , J. Fjeldstad et al., proceedings FLEXCON™ '95.

[2] "High Speed Ultraviolet Laser Via Formation on Flex and Chip Scale Packages", Alan Cable, proceedings FLEXCON™ '96.

[3] "High Density SMT Assemblies Based on Flex Substrates" , Robert Larmouth and James Keating, proceedings SMI '96.

[4] "High Density Z-axis Colamination for Double Sided MCM-L Substrates in 3-D Stacked Missile Electronics", P. Drake et. al., proceedings FLEXCON™ '96.

[5] "High Density Multilayer Interconnect Based on Adhesiveless Flex Circuits" , Craig Ernsberger, proceedings FLEXCON™ '94.

[6] "Reliability of micro-BGA-on-Flex Assemblies" , Robert Larmouth and James Keating, proceedings SMI '97.

ABOUT THE AUTHORS:

James Keating is Manager, Advanced Projects at Teledyne Electronic Technologies, Printed Circuit Technology, where he has worked since 1988. During this time he has held positions in Engineering and Technical Marketing. Jim has over twelve years experience in the development, manufacture, and application of flex and rigid flex circuitry. He holds a B. S. in Manufacturing Engineering from Wentworth Institute of Technology in Boston, MA.

Robert Larmouth is Director, Advanced Development at Teledyne Electronic Technologies, where he has worked since 1994. Prior to that, he was employed at Digital Equipment Corporation for over ten years, most recently as Engineering Manager. Bob has over 18 years of experience in electronics packaging and assembly technology. He holds a B. S. in Materials Engineering from Wilkes University and an M. S. in Materials Science from the University of Virginia.